

FIG 1A DLL and NCDL mechanism in DDR memory controller

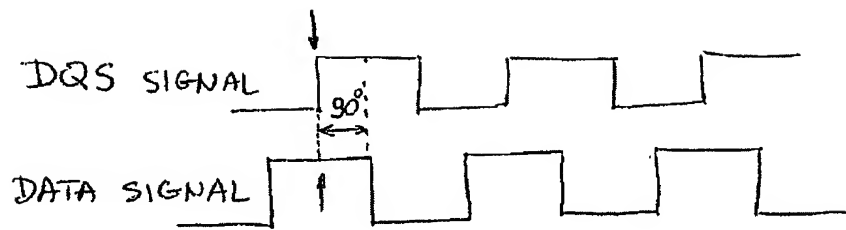


FIG. 1B: CENTER
ALIGNMENT OF DQS AND
DATA SIGNALS

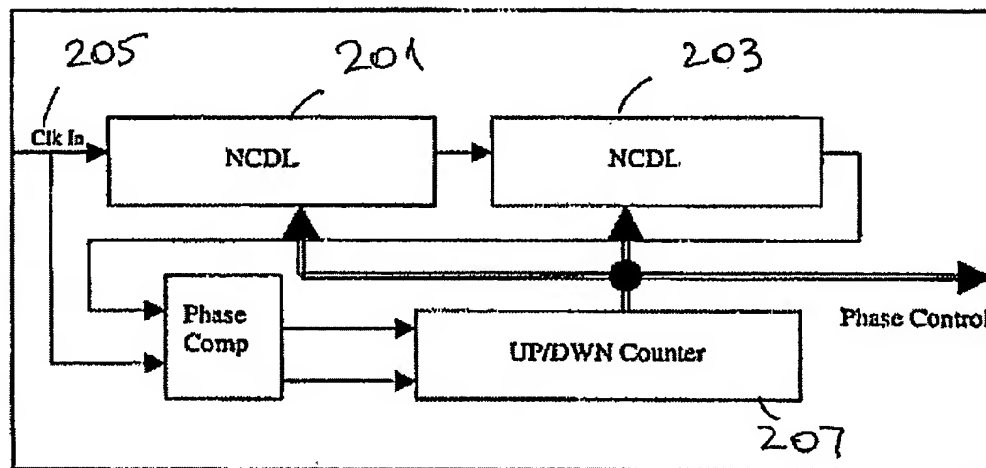


FIG 2: Delay Locked Loop

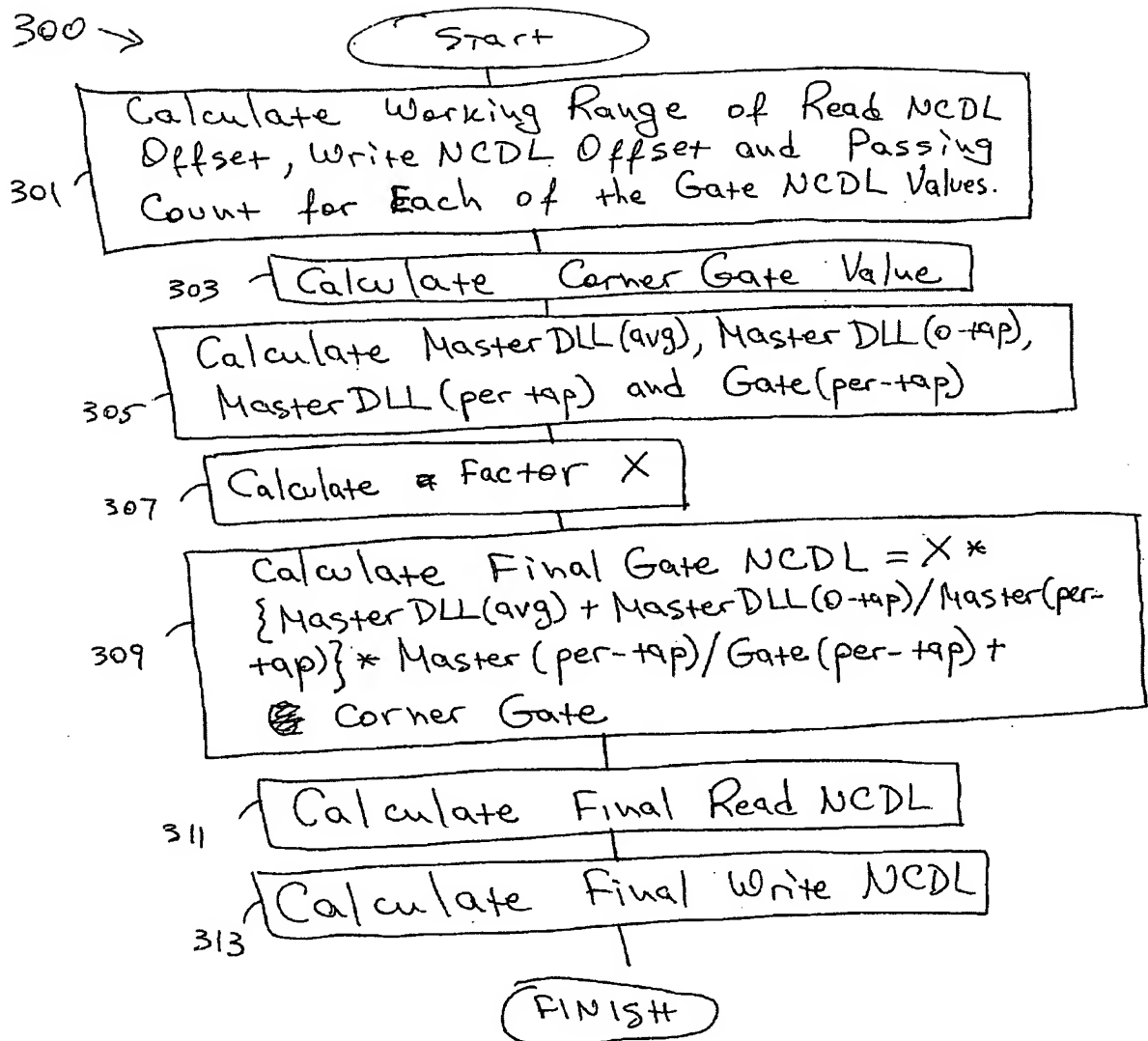


FIG. 3

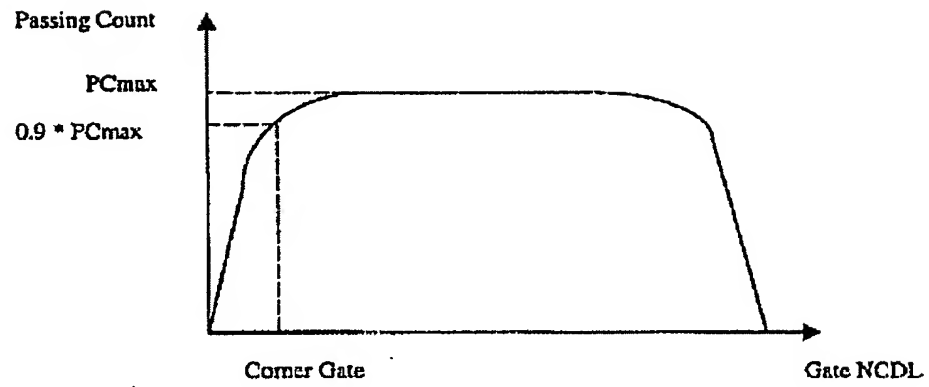


FIG.4: Plot of Passing Count Vs Gate NCDL

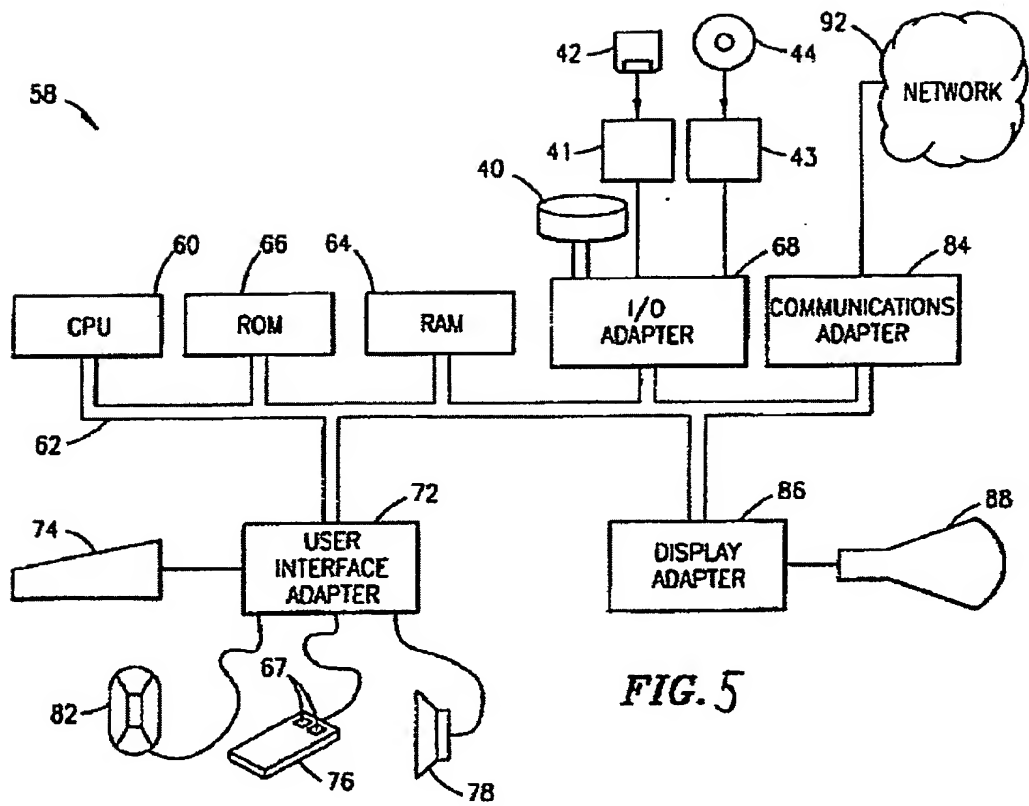


FIG. 5